FAIRCHILD
SEMICONDUCTOR®

September 2002

PWM Optimized

ISL9N303AP3 / ISL9N303AS3ST / ISL9N303AS3

N-Channel Logic Level UltraFET® Trench MOSFETs
30V, 75A, 3.2mΩ

General Description

This device employs a new advanced trench MOSFET technology and features low gate charge while maintaining low on-resistance.

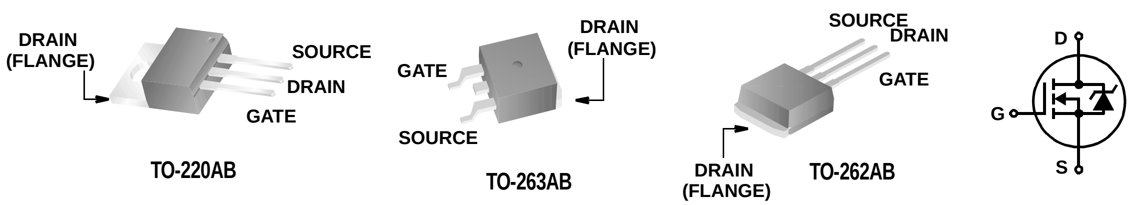
Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

Applications

- DC/DC converters

Features

- Fast switching
- $r_{DS(ON)}$ = 0.0026Ω (Typ), V_{GS} = 10V
- $r_{DS(ON)}$ = 0.004Ω (Typ), V_{GS} = 4.5V
- Q_g (Typ) = 61nC, V_{GS} = 5V
- Q_{gd} (Typ) = 17nC
- C_{ISS} (Typ) = 7000pF



MOSFET Maximum Ratings T_C= 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_C = 25°C, V_{GS} = 10V)	75	A
	Continuous (T_C = 100°C, V_{GS} = 4.5V)	75	A
	Continuous (T_C = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 43°C/W)	25	A
	Pulsed	Figure 4	
P_D	Power dissipation Derate above	215 1.43	W W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220, TO-262, TO-263	0.7	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220, TO-262, TO-263	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in^2 copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
N303AS	ISL9N303AS3ST	TO-263AB	330mm	24mm	800 units
N303AP	ISL9N303AP3	TO-220AB	Tube	N/A	50 units
N303AS	ISL9N303AS3	TO-262AA	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 25V, V_{GS} = 0V, T_C = 150°C	-	-	250	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250µA	1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 75A, V_{GS} = 10V	-	0.0026	0.0032	Ω
		I_D = 75A, V_{GS} = 4.5V	-	0.004	0.005	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	7000	-	pF
C_{OSS}	Output Capacitance		-	1350	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	570	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 75A, I_g = 1.0mA		115	172	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V	-	61	92	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V	-	6.5	9.8	nC
Q_{gs}	Gate to Source Gate Charge		-	14	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	17	-	nC
Switching Characteristics (V_{GS} = 4.5V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 24A, V_{GS} = 4.5V, R_G = 2.4Ω	-	-	155	ns
$t_{d(ON)}$	Turn-On Delay Time		-	22	-	ns
t_r	Rise Time		-	80	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	35	-	ns
t_f	Fall Time		-	25	-	ns
t_{OFF}	Turn-Off Time		-	-	90	ns
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 24A, V_{GS} = 10V, R_G = 2.4Ω	-	-	123	ns
$t_{d(ON)}$	Turn-On Delay Time		-	12	-	ns
t_r	Rise Time		-	69	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	51	-	ns
t_f	Fall Time		-	21	-	ns
t_{OFF}	Turn-Off Time		-	-	107	ns
Unclamped Inductive Switching						
t_{AV}	Avalanche Time	I_D = 4.1A L = 3.0 mH	275	-	-	µs
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 75A	-	-	1.25	V
		I_{SD} = 35A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	31	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75A, dI_{SD}/dt = 100A/µs	-	-	20	nC

Typical Characteristics

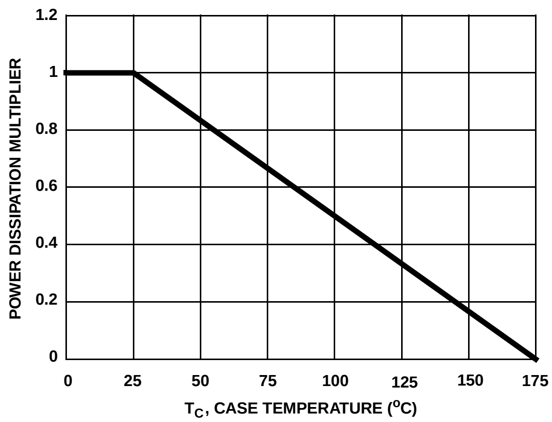


Figure 1. Normalized Power Dissipation vs Ambient Temperature

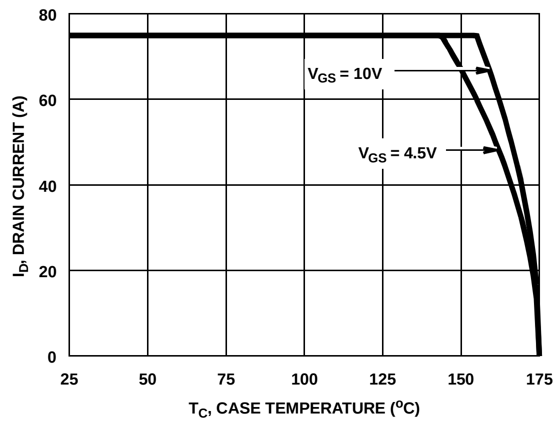


Figure 2. Maximum Continuous Drain Current vs Case Temperature

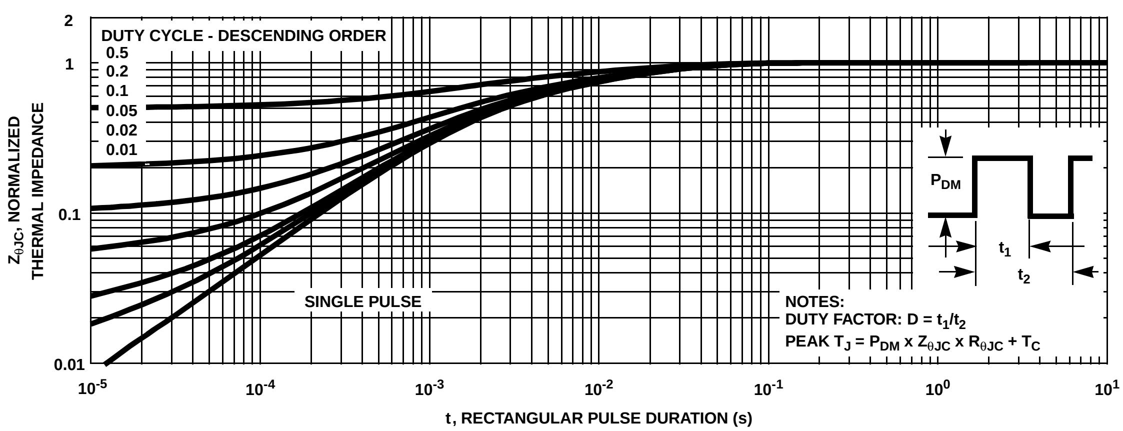


Figure 3. Normalized Maximum Transient Thermal Impedance

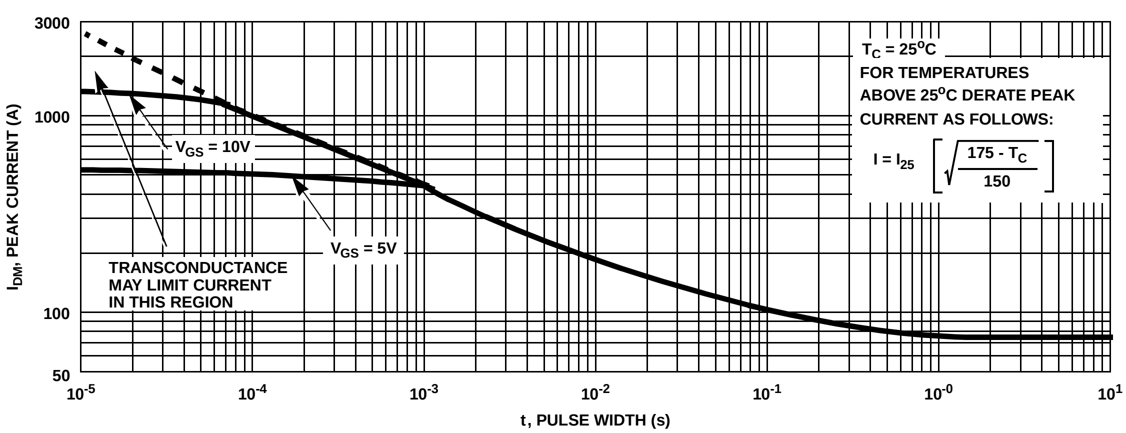


Figure 4. Peak Current Capability

Typical Characteristics

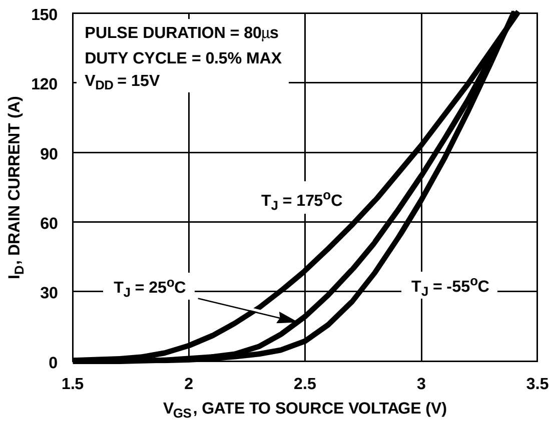


Figure 5. Transfer Characteristics

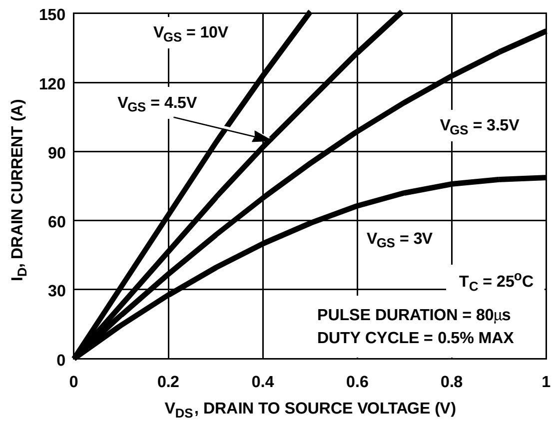


Figure 6. Saturation Characteristics

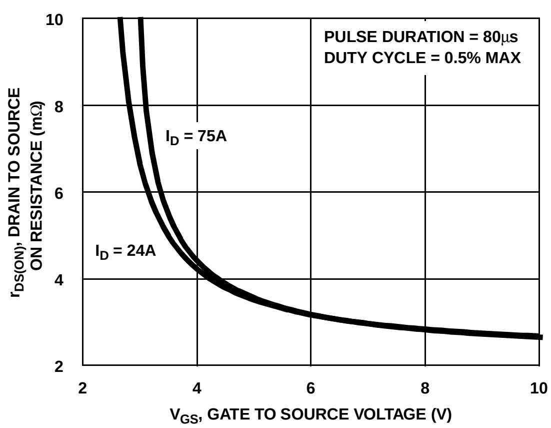


Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current

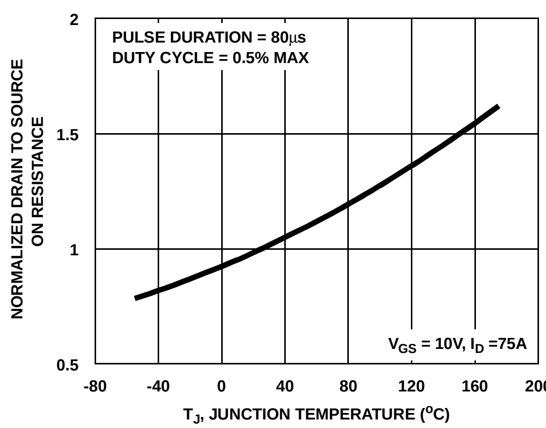


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

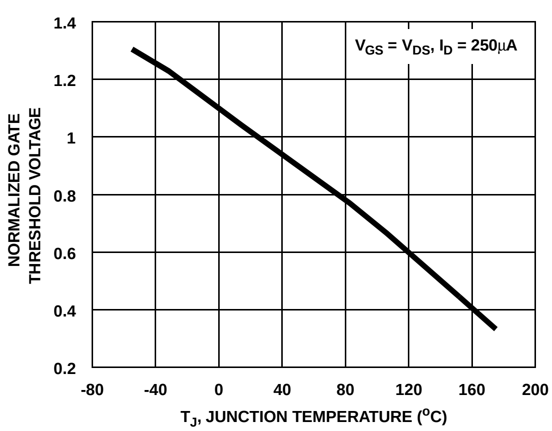


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

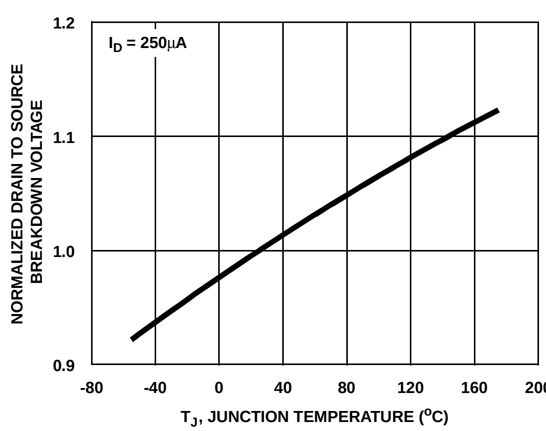


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristics

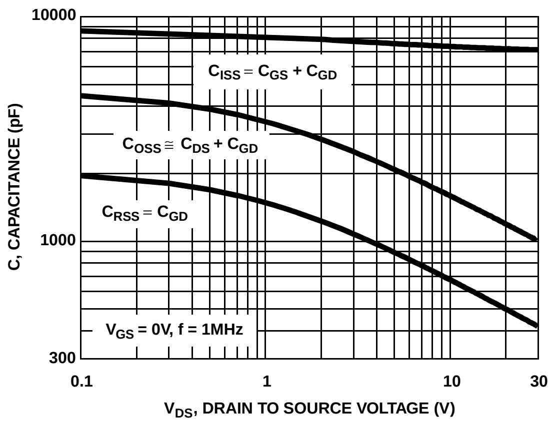


Figure 11. Capacitance vs Drain to Source Voltage

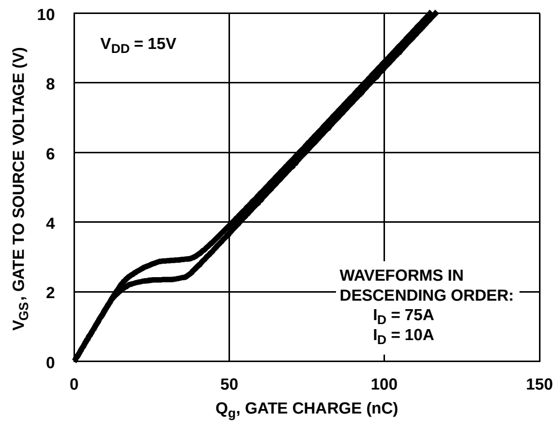


Figure 12. Gate Charge Waveforms for Constant Gate Currents

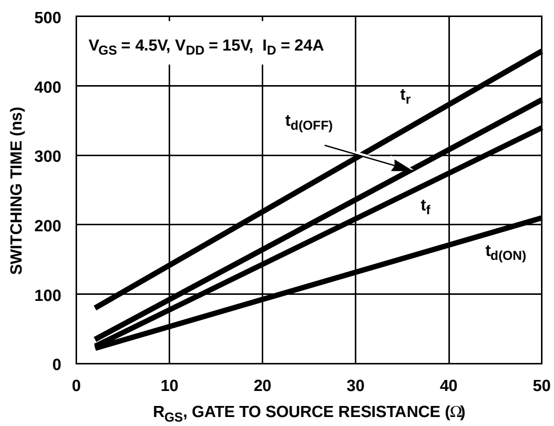


Figure 13. Switching Time vs Gate Resistance

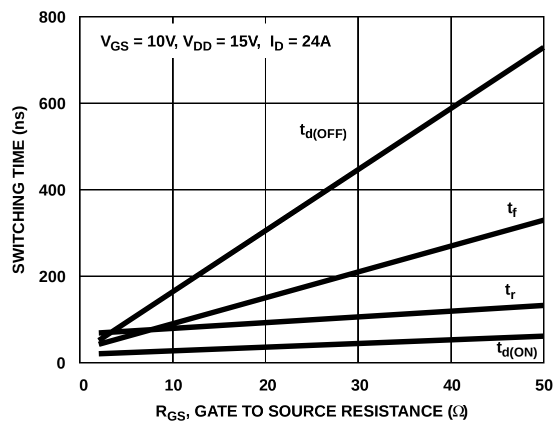


Figure 14. Switching Time vs Gate Resistance

Test Circuits and Waveforms

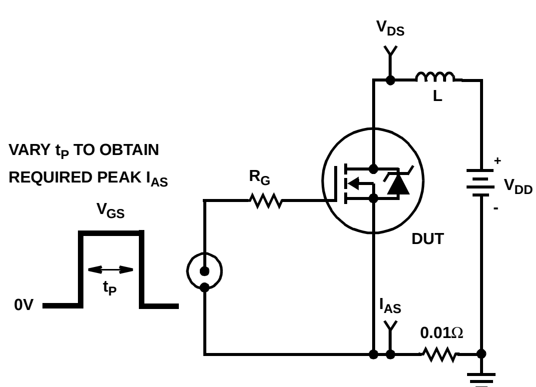


Figure 15. Unclamped Energy Test Circuit

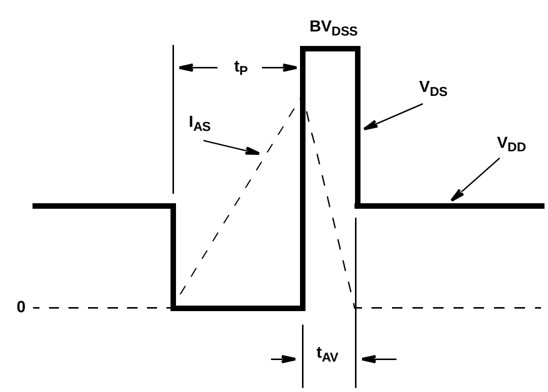


Figure 16. Unclamped Energy Waveforms

Test Circuits and Waveforms (Continued)

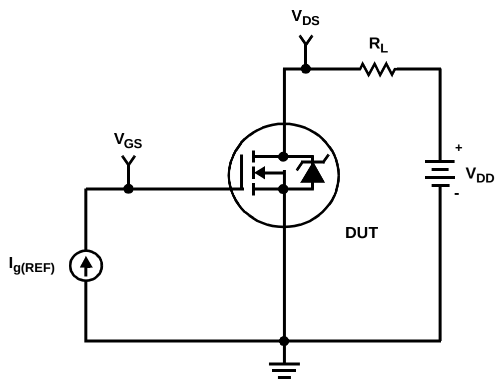


Figure 17. Gate Charge Test Circuit

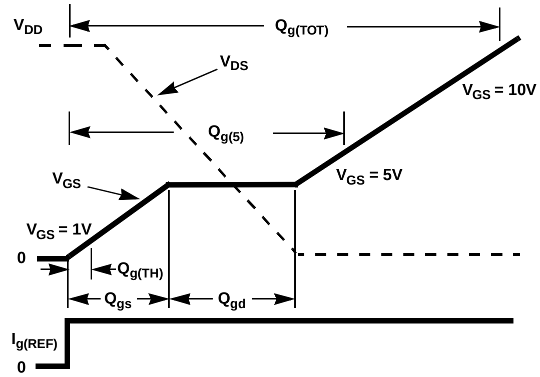


Figure 18. Gate Charge Waveforms

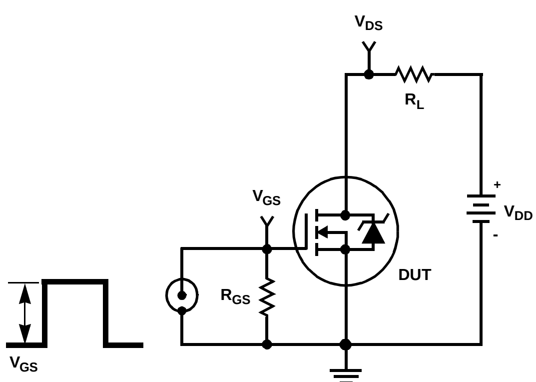


Figure 19. Switching Time Test Circuit

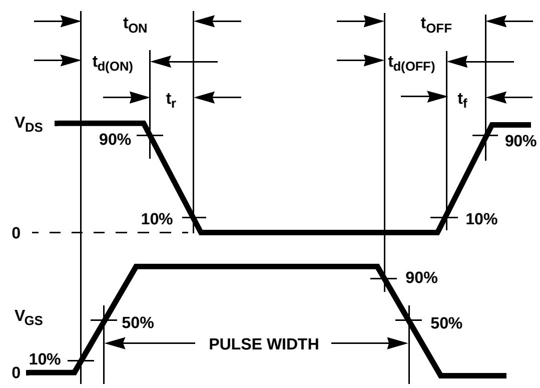


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \qquad \text{(EQ. 2)}$$

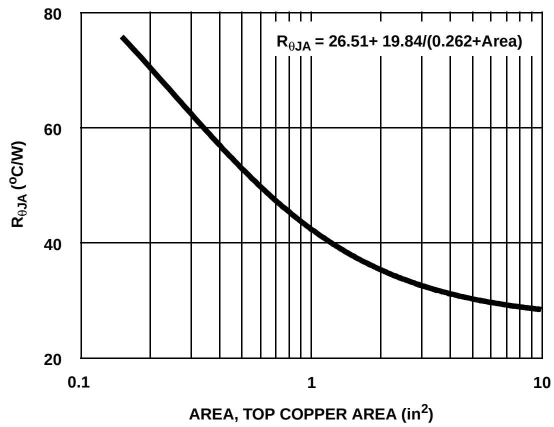
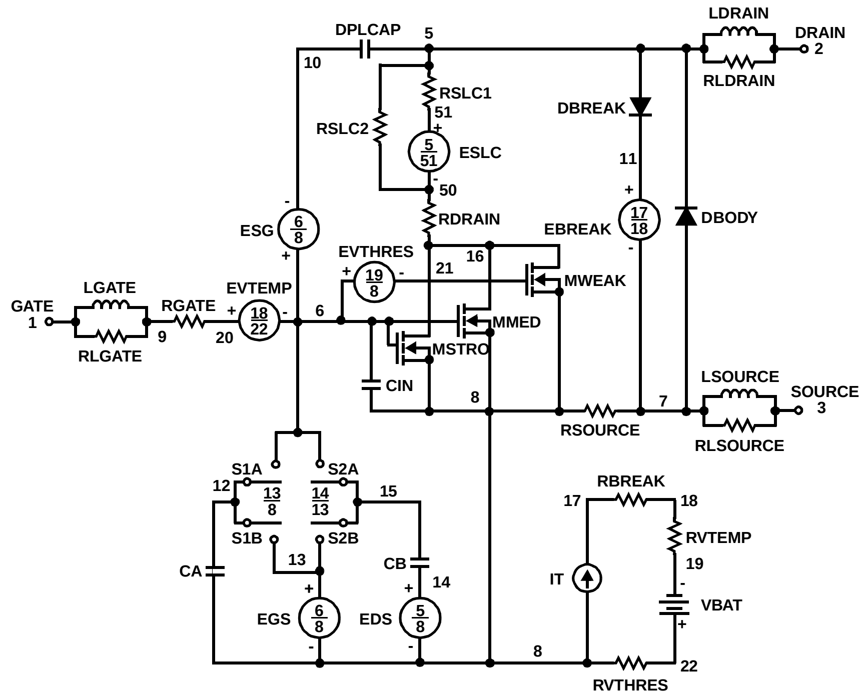


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model




```
.SUBCKT ISL9N303AP3 2 1 3 ;        rev May 2001
Ca  12  8 6.3e-9
Cb 15 14 3.8e-9
Cin 6 8 6.7e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 30.6
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.618e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 1.98e-9

RLgate 1 9 56.1
RLdrain 2 5 15
RLsource 3 7 19.8

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 0.9e-3
Rgate 9 20 0.639
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 1.8e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*500),3))}

.MODEL DbodyMOD D (IS=8e-11 N=1.06 RS=2.3e-3 TRS1=1.1e-3 TRS2=3e-6
+ CJO=2.6e-9 M=0.43 TT=3e-10 XTI=0.1)
.MODEL DbreakMOD D (RS=0.3 TRS1=1.8e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=2.05e-9 IS=1e-30 N=10 M=0.46)

.MODEL MstroMOD NMOS (VTO=2.16 KP=270 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=1.65 KP=20 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=0.639)
.MODEL MweakMOD NMOS (VTO=1.29 KP=0.1 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=6.39 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.05e-3 TC2=-7e-7)
.MODEL RdrainMOD RES (TC1=1e-2 TC2=1.8e-5)
.MODEL RSLCMOD RES (TC1=3.5e-4 TC2=5e-6)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-3e-3 TC2=-11e-6)
.MODEL RvtempMOD RES (TC1=-1.5e-3 TC2=1.4e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-4)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.9 VOFF=0.2)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.2 VOFF=-0.9)
.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV May 20011
template ISL9N303AP3 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=8e-11,nl=1.06,rs=2.3e-3,trs1=1.1e-3,trs2=3e-6,cjo=2.6e-9,m=0.43,tt=3e-10,xti=0.1)
dp..model dbreakmod = (rs=0.3,trs1=1.8e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=2.05e-9,isl=10e-30,nl=10,m=0.46)
m..model mstrongmod = (type=_n,vto=2.16,kp=270,is=1e-30, tox=1)
m..model mmedmod = (type=_n,vto=1.65,kp=20,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.29,kp=0.1,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-5,voff=-4)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-4,voff=-5)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.9,voff=0.2)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.2,voff=-0.9)
c.ca n12 n8 = 6.3e-9
c.cb n15 n14 = 3.8e-9
c.cin n6 n8 = 6.7e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 30.6
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

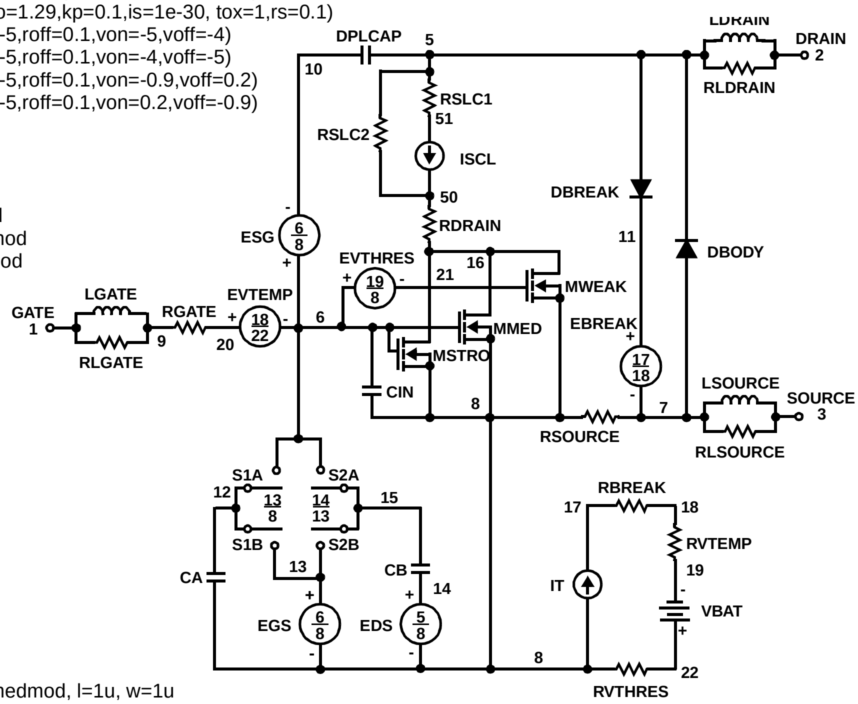
l.lgate n1 n9 = 5.618e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 1.98e-9

res.rlgate n1 n9 = 56.1
res.rldrain n2 n5 = 15
res.rlsource n3 n7 = 19.8

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.05e-3,tc2=-7e-7
res.rdrain n50 n16 = 0.9e-3, tc1=1e-2,tc2=1.8e-5
res.rgate n9 n20 = 0.639
res.rslc1 n5 n51 = 1e-6, tc1=3.5e-4,tc2=5e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.8e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-3e-3,tc2=-11e-6
res.rvtemp n18 n19 = 1, tc1=-1.5e-3,tc2=1.4e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/500))** 3))
}



SPICE Thermal Model

REV May 2001

ISL9N303AP3

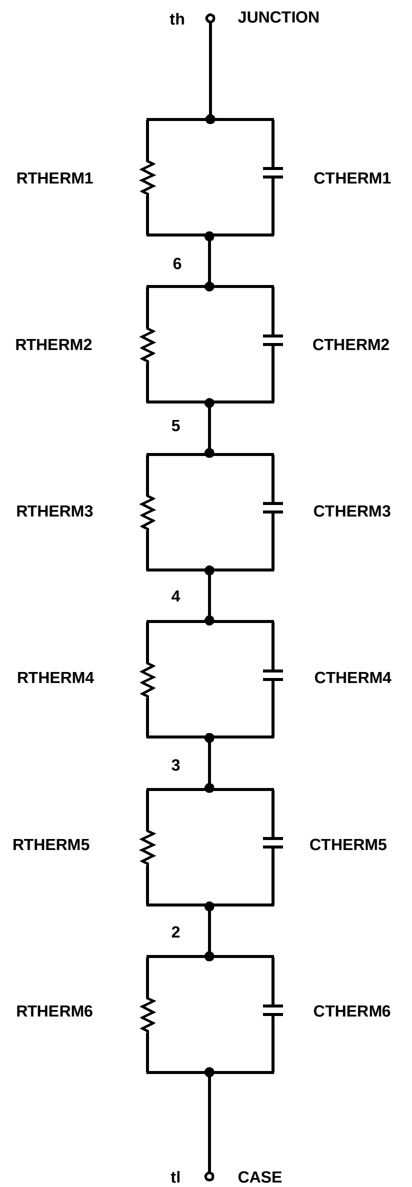
CTHERM1 TH 6 3.9e-3
CTHERM2 6 5 7.1e-3
CTHERM3 5 4 8.7e-3
CTHERM4 4 3 9.6e-3
CTHERM5 3 2 1e-2
CTHERM6 2 TL 2.4e-2

RTHERM1 TH 6 3.9e-5
RTHERM2 6 5 7.5e-4
RTHERM3 5 4 4.8e-3
RTHERM4 4 3 2.7e-2
RTHERM5 3 2 1.6e-1
RTHERM6 2 TL 3.7e-1

SABER Thermal Model

```
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thermal_c th, tl
{
ctherm.ctherm1 th 6 =3.9e-3
ctherm.ctherm2 6 5 =7.1e-3
ctherm.ctherm3 5 4 =8.7e-3
ctherm.ctherm4 4 3 =9.6e-3
ctherm.ctherm5 3 2 =1e-2
ctherm.ctherm6 2 tl =2.4e-2

rtherm.rtherm1 th 6 =3.9e-5
rtherm.rtherm2 6 5 =7.5e-4
rtherm.rtherm3 5 4 =4.8e-3
rtherm.rtherm4 4 3 =2.7e-2
rtherm.rtherm5 3 2 =1.6e-1
rtherm.rtherm6 2 tl =3.7e-1
}
```



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ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E^2CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.